

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first conductivity type base layer;

5 a second conductivity type base layer selectively
formed on an upper surface of said first conductivity
type base layer;

a first conductivity type emitter layer
selectively formed on a surface of said second
conductivity type base layer;

10 a gate electrode formed on a part of said second
conductivity type base layer sandwiched between said
first conductivity type emitter layer and said first
conductivity type base layer, with a gate insulating
film interposed between said second conductivity type
15 base layer and said gate electrode;

a first conductivity type buffer layer formed on
a back surface of said first conductivity type base
layer; and

20 a second conductivity type collector layer formed
on a back surface of said first conductivity type
buffer layer, wherein

a requirement of $d_2/d_1 > 1.5$ is satisfied, where
 d_1 is a depth in said first conductivity type buffer
layer, as measured from an interface of said first
25 conductivity type buffer layer and said second
conductivity type collector layer, at which a
concentration of a first conductivity type activated

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impurity in said first conductivity type buffer layer shows a peak value, and d2 is a shallowest depth in said first conductivity type buffer layer, as measured from the interface of said first conductivity type
5 buffer layer and said second conductivity type collector layer, at which an activation ratio of said first conductivity type impurity in said first conductivity type buffer layer is a predetermined value.

10 2. The semiconductor device according to claim 1, wherein said activation ratio is defined by a concentration of activated those of said first conductivity type impurity in said first conductivity type buffer layer/a concentration of said first
15 conductivity type impurity in said first conductivity type buffer layer.

3. The semiconductor device according to claim 2, wherein said concentration of said activated first conductivity type impurity in said first conductivity type buffer layer is observed by a Spreading Resistance
20 analysis and said concentration of said first conductivity type impurity in said first conductivity type buffer layer is observed by a Secondary Ion Mass Spectrometry analysis.

25 4. The semiconductor device according to claim 1, wherein said predetermined value for said activation ratio is substantially 0.3 or lower than 0.3.

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5. The semiconductor device according to claim 1, wherein said first conductivity type buffer layer and said second conductivity type collector layer are formed from impurity diffusion layers.

5 6. The semiconductor device according to claim 2, wherein said first conductivity type buffer layer and said second conductivity type collector layer are formed from impurity diffusion layers.

10 7. The semiconductor device according to claim 1, wherein said first conductivity type buffer layer and said second conductivity type collector layer are formed by implanting impurities into and annealing a first conductivity type semiconductor wafer having a substantially uniform impurity concentration.

15 8. The semiconductor device according to claim 2, wherein said first conductivity type buffer layer and said second conductivity type collector layer are formed by implanting impurities into and annealing a first conductivity type semiconductor wafer having a substantially uniform impurity concentration.

20 9. The semiconductor device according to claim 1, wherein

 said first conductivity type base layer, said second conductivity type base layer, said first conductivity type emitter layer, said first conductivity type buffer layer and said second conductivity type collector layer are formed from

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impurity diffusion layers.

10. The semiconductor device according to claim 2,
wherein

said first conductivity type base layer, said
5 second conductivity type base layer, said first
conductivity type emitter layer, said first
conductivity type buffer layer and said second
conductivity type collector layer are formed from
impurity diffusion layers.

10 11. The semiconductor device according to claim 1,
wherein said first conductivity type base layer, said
second conductivity type base layer and said first
conductivity type emitter layer are formed by
implanting impurities into a first conductivity type
15 semiconductor wafer having a substantially uniform
impurity concentration, and said first conductivity
type buffer layer and said second conductivity type
collector layer are formed by implanting impurities
into and annealing said semiconductor wafer.

20 12. The semiconductor device according to claim 2,
wherein said first conductivity type base layer, said
second conductivity type base layer and said first
conductivity type emitter layer are formed by
implanting impurities into a first conductivity type
25 semiconductor wafer having a substantially uniform
impurity concentration, and said first conductivity
type buffer layer and said second conductivity type

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collector layer are formed by implanting impurities into and annealing said semiconductor wafer.

13. The semiconductor device according to claim 1, wherein said depth d2 is larger than said depth d1.

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